PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

United States Patent and Trademark Office
(Box PCT)
Crystal Plaza 2
Washington, DC 20231
ETATS-UNIS D'AMERIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 31 March 1998 (31.03.98)	
International application No. PCT/JP97/03267	**Applicant's or agent's file reference** E3482-00
International filing date (day/month/year) 16 September 1997 (16.09.97)	**Priority date** (day/month/year) 17 September 1996 (17.09.96)
Applicant MIURA, Hideo et al	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

10 March 1998 (10.03.98)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO
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1211 Geneva 20, Switzerland
Facsimile No.: (41-22) 740.14.35

Authorized officer

M. Sakai

Telephone No.: (41-22) 338.83.38

4

PATENT COOPERATION TREATY

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INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (PCT/IPEA/416)
81-52.631PCT-mo.		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/JP97/03267	16/09/1997	17/09/1996
International Patent Classification (IPC) or national classification and IPC		
H01L21/762		
Applicant		
HITACHI, LTD. et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 8 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 1 sheets.

3. This report contains indications relating to the following items:

I	☒	Basis of the report
II	☐	Priority
III	☐	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
IV	☐	Lack of unity of invention
V	☒	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
VI	☐	Certain documents cited
VII	☒	Certain defects in the international application
VIII	☒	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
10/03/1998	22.12.98
Name and mailing address of the IPEA/	Authorized officer
European Patent Office D-80298 Munich Tel. (+49-89) 2399-0, Tx: 523656 epmu d Fax: (+49-89) 2399-4465	Krause, J Telephone No. (+49-89) 2399-2829

Form PCT/IPEA/409 (Cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/JP97/03267

I. Basis of the r port

1. This report has been drawn on the basis of (*substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments.*):

Description, pages:

1-28	as originally filed				

Claims, No.:

2-8	as originally filed				
1	as received on	19/11/1998	with letter of	18/11/1998	

Drawings, sheets:

1/9-9/9	as originally filed

2. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:
- ☐ the drawings, sheets:

3. ☐ This report has been established as if (some of) the amendments had not been made, since they have be n considered to go beyond the disclosure as filed (Rule 70.2(c)):

4. Additional observations, if necessary:

V. R asoned stat ment under Article 35(2) with regard to novelty, inventiv step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1, 3, 5, 6
	No:	Claims	2, 4, 7, 8
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1 - 8
Industrial applicability (IA)	Yes:	Claims	1 - 8
	No:	Claims	

2. Citations and explanations

see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Concerning Section V:

I. Claim 1:

1. The document US-A-5 236 861 (= D3) describes a method of fabricating a semiconductor device (cf. column 3, line 43, to column 4, line 62, and Figs 3A-3E) comprising the steps of

   (a) forming an oxidation prevention film (2) on a circuit formation surface of a semiconductor substrate (1);

   (b) forming trench regions (6) in said substrate from said circuit formation surface thereof;

   (d) forming an insulating film (9) inside said oxidised trench regions so as to completely fill them; and

   (e) performing a second oxidation to selectively oxidise the opening side of said completely filled trench regions in said substrate.

2. The subject-matter of claim 1 differs therefrom only in that a first oxidation step (c) is performed prior to filling the trench regions to form an oxide film on said trench regions formed in step (b).

3. An oxidation step to form a oxide film on the inside of the trench regions is known from the document US-A-5 536 675 (= D1), which belongs to the same narrow technical field (cf. column 5, line 11, to column 7, line 62, and Fig. 3E). It is clearly stated in D1 that the first oxidation improves the surface quality inside the trenches (cf. in particular column 5, line 66, to column 6, line 2, and column 6, lines 45 to 48). The person skilled in the art would therefore routinely consult document D1 and obtain a method with all the features of claim 1 without employment of inventive skill.

4. The arguments of the applicant put forward in his letter of 19 November 1998 are not convincing because the second oxidation step is performed for the whole substrate surface also according to the present application (cf. page 14, line 4, to page 15, line 10). The selectivity of the oxidation is due to the oxidation preventing film, which is also present in D3. Thus there is no difference between step (e) of claim 1 and the corresponding step in the method of document D3.

Furthermore, it should be mentioned that oxide formation at other parts of the substrate surface than the trench regions is not excluded by the present wording of claim 1.

5. Claim 1 is therefore not considered to meet the requirement of Article 33(3) PCT.

II. Claims 2 and 3:

1. The document D1 describes a method of fabricating a semiconductor device comprising the steps of
   (a) forming an oxidation prevention film (220) on a circuit formation surface of a semiconductor substrate (200);
   (b) forming shallow trenches (241, 252a), which must have a radius of curvature at corners, in a desired position of the circuit formation surface of said semiconductor substrate (200);
   (c) forming a trench (242b) having a predetermined depth to said shallow trenches having a radius of curvature so formed;
   (d) oxidizing said trench portions (251, 252a, 252b) formed in said semiconductor substrate;
   (e) burying a buried insulating film (260) into said trenches so oxidised;
   (f) removing said buried insulating film (260) formed on said oxidation preventing film (220); and
   (g) removing said oxidation preventing film (220) formed on the circuit formation surface of said circuit substrate (200).

Thus all the features of claim 2 are known from document D1. As a consequence, claim 2 is also not considered to meet the requirements of Article 33(2) and (3) PCT.

2. The document EP-A-0 459 397 (= D2) describes a method of forming a shallow trench by isotropic etching and a deep trench by anisotropic etching after an oxidation preventing film (23) has been deposited (cf. column 2, line 39, to column 3, line 16, and Figs 2A-2D). The person skilled in the art would routinely consult document D2, which belongs to the same narrow technical field as document D1, and obtain a method with all the features of claim 3 without employment of inventive skill.

As a consequence, claim 3 is not considered to meet the requirement of Article 33(3) PCT.

III. Claim 4:

1. The document D3 describes a method of fabricating a semiconductor device, which comprises the steps of
(a) forming an oxidation prevention film (2) on a circuit formation surface of a semiconductor substrate (1);
(b) forming trenches (6) having a predetermined depth at desired positions of the circuit formation surface of said semiconductor substrate (1);
(c) oxidising said trench portions (6) formed in said semiconductor substrate (1); therewith
(d) burying a buried insulating film (9) into said trenches so oxidised;
(e) removing said buried insulating film (9) formed on said oxidation prevention film (2);
(f) oxidising said semiconductor substrate (1) after said buried insulating film formed on said oxidation prevention film (2) is removed; and
(g) removing said oxidation prevention film (2) formed on the circuit formation surface of said semiconductor substrate.

2. As a consequence, all the features of claim 4 are anticipated by document D3, and claim 4 is not considered to meet the requirements of Article 33(2) and (3) PCT, accordingly.

IV. Claims 5 and 6:

1. Claim 5 comprises all the method steps of claim 2, with the exception that a plurality of deep trenches having a predetermined depth in the shallow trenches are formed. Furthermore, claim 5 comprises the step (g), which corresponds to step (f) of claim 4.

2. The person skilled in the art would be aware of document D3, which belongs to the

same narrow field as D1, and routinely apply the second oxidation step after removal of the buried insulating layer outside the trenches. In document D3 a plurality of trenches are formed in a substrate, and the skilled person would also apply the method of D1 in this sense to provide insulation trenches for more than one semiconductor device.

3. As a consequence, he would obtain a method with all the features of claim 5 without employment of inventive skill. Claim 5 is therefore not considered to meet the requirement of Article 33(3) PCT.

4. The additional feature of claim 6 is known from document D2 and would be routinely applied in a method according to D1 or D3. Thus claim 6 is also not considered to meet the requirement of Article 33(3) PCT.

IV. Claims 7 and 8:

1. Document D3 describes a semiconductor device (cf. Fig. F and the text cited above) of the type wherein a device isolation oxide film structure formed on a circuit formation surface of a semiconductor substrate (1) is a trench isolation structure and an angle θ of a trench, which constitutes said trench isolation structure with the circuit formation surface of said semiconductor substrate, in a depth-wise direction with respect to the side surface of said semiconductor substrate is within the range $90° < \theta < 180°$, and a silicon oxide (9) exists inside said trench (6).

2. As a consequence, all the features of claims 7 and 8 are anticipated by document D3. Claims 7 and 8 are therefore not considered to meet the requirements of Article 33(2) and (3) PCT.

Conc rning S ction VII:

1. To meet the requirements of Rule 5.1(a)(ii) PCT, the documents D1, D2, and D3 should be identified in the description and the relevant background art disclosed therein should be briefly discussed.

2. The features of claims 2 to 8 are not provided with reference signs placed in parentheses (Rule 6.2(b) PCT).

Concerning Section VIII:

1. Although claims 1, 2, 4, 5, 7, and 8 have been drafted as separate independent claims, they appear to relate effectively to the same subject-matter and to differ from each other only with regard to the definition of the subject-matter for which protection is sought and in respect of the terminology used for the features of that subject-matter. The aforementioned claims therefore lack conciseness. Moreover, lack of clarity of the claims as a whole arises, since the plurality of independent claims makes it difficult, if not impossible, to determine the matter for which protection is sought, and places an undue burden on others seeking to establish the extent of the protection.

   Hence, claims 1, 2, 4, 5, 7, and 8 do not meet the requirements of Article 6 PCT.

   In order to overcome this objection, it would appear appropriate to file an amended set of claims defining the relevant subject-matter in terms of a single independent claim in each category followed by dependent claims covering features which are merely optional (Rule 6.4 PCT).

2. The definitions of the radius of curvature in claims 2 and 5 and of the angle θ in claims 7 and 8 are not understandable (Article 6 PCT).

Patentanwälte
BEETZ & PARTNER
Steinsdorfstr. 10, D-80538 München

New Claim 1
==========

1. A method of fabricating a semiconductor device comprising the steps of

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (1),

(b) forming trench regions in said substrate from said circuit formation surface thereof,

(c) performing a first oxidation to form an oxide film (5) on said trench regions formed in step (b),
and

(d) forming an insulating film (9) inside said oxidised trench regions so as to completely fill them,

characterised by a further step of

(e) performing a second oxidation to selectively oxidise the opening side (12) of said completely filled trench regions in said substrate (1).

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
E3482-00		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/JP 97/ 03267	16/09/1997	17/09/1996
Applicant		
HITACHI, LTD. et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. [ ] **Certain claims were found unsearchable** (see Box I).

2. [ ] **Unity of invention is lacking** (see Box II).

3. [ ] The international application contains disclosure of a **nucleotide and/or amino acid sequence listing** and the international search was carried out on the basis of the sequence listing
   - [ ] filed with the international application.
   - [ ] furnished by the applicant separately from the international application,
     - [ ] but not accompanied by a statement to the effect that it did not include matter going beyond the disclosure in the international application as filed.
   - [ ] Transcribed by this Authority

4. With regard to the **title,**
   - [X] the text is approved as submitted by the applicant
   - [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   - [X] the text is approved as submitted by the applicant
   - [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this International Search Report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is:
   Figure No. 2E-2I
   - [X] as suggested by the applicant.
   - [ ] because the applicant failed to suggest a figure.
   - [ ] because this figure better characterizes the invention.
   - [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP 97/03267

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/762

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 536 675 A (BOHR MARK T) 16 July 1996 see column 5, line 11 - column 8, line 6; figures 1,3A-3E	1,2
Y	see column 5, line 26 - line 31	3,6
Y		4,5

Y	US 5 236 861 A (OTSU TAKAJI) 17 August 1993 see column 3, line 43 - column 4, line 58; figures 3A-3F	4,5

Y	EP 0 459 397 A (TOKYO SHIBAURA ELECTRIC CO) 4 December 1991 see column 2, line 39 - column 3, line 16; figures 2A-2H	3,6

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
8 December 1997	19/12/1997

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Vancraeynest, F

Form PCT/ISA/210 (second sheet) (July 1992)

Inte[redacted]al Application No
PCT/JP 97/03267

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 839 306 A (WAKAMATSU HIDETOSHI) 13 June 1989 see column 1, line 57 - column 3, line 11; example 1E	7,8
A	US 5 316 965 A (PHILIPOSSIAN ARA ET AL) 31 May 1994 see column 3, line 27 - column 4, line 64; figures 5-7	1,4
A	EP 0 660 391 A (TOKYO SHIBAURA ELECTRIC CO) 28 June 1995 see figures 6A-7	1,2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/JP 97/03267

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5536675 A	16-07-96	NONE	
US 5236861 A	17-08-93	JP 5047919 A	26-02-93
EP 0459397 A	04-12-91	JP 2575520 B	29-01-97
		JP 4030556 A	03-02-92
		JP 4030557 A	03-02-92
		KR 9606714 B	22-05-96
		US 5434447 A	18-07-95
		US 5683908 A	04-11-97
US 4839306 A	13-06-89	JP 63234534 A	29-09-88
US 5316965 A	31-05-94	NONE	
EP 0660391 A	28-06-95	JP 7176604 A	14-07-95
		US 5578518 A	26-11-96

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D INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H01L 21/762

A1

(11) International Publication Number: WO 98/12742

(43) International Publication Date: 26 March 1998 (26.03.98)

(21) International Application Number: PCT/JP97/03267

(22) International Filing Date: 16 September 1997 (16.09.97)

(30) Priority Data:
8/244445 17 September 1996 (17.09.96) JP

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(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: MIURA, Hideo [JP/JP]; 8-9-512, Minamikoshigaya 4-chome, Koshigaya-shi, Saitama 343 (JP). KITANO, Makoto [JP/JP]; 1057-8, Shiratorimachi, Tsuchiura-shi, Ibaraki 300 (JP). IKEDA, Shuji [JP/JP]; 30-8, Nukuikitamachi 3-chome, Koganei-shi, Tokyo 184 (JP). SUZUKI, Norio [JP/JP]; 1-1, Atagocho, Mito-shi, Ibaraki 310 (JP).

(74) Agents: ASAMURA, Kiyoshi et al.; New Ohtemachi Building, Room 331, 2-1, Ohtemachi 2-chome, Chiyoda-ku, Tokyo 100 (JP).

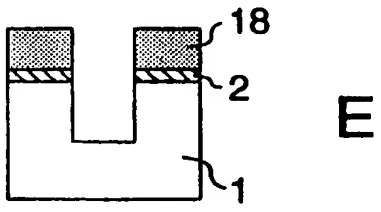
(81) Designated States: CN, KR, SG, US, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

(57) Abstract

In a semiconductor device having a trench isolation structure, after a trench surface is selectively oxidized by a conventional method, an oxidation prevention film is removed, the entire surface of the substrate is again oxidized while only an oxide film on the substrate or trench surface is exposed, and a radius of curvature is provided to the shape of the oxide film near the trench upper end portion.



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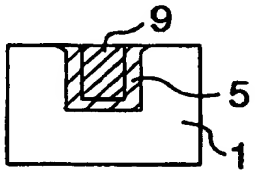

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DESCRIPTION

SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

TECHNICAL FIELD

This invention relates to a semiconductor device having a trench isolation structure having high reliability, and a method of fabricating the same.

BACKGROUND ART

A LOCOS (Local Oxidation of Silicon) structure is known as a structure for electrically insulating and isolating adjacent devices on a semiconductor substrate. This structure is formed by selectively oxidizing a substrate surface to form a thick thermal oxide film, and has been employed in various semiconductor devices. However, because this LOCOS structure has low processing accuracy, it is not suitable for an insulation/isolation structure of high integration semiconductor devices such as deep submicron devices in which high processing dimensional accuracy is required for the thermal oxide film. Therefore, a so-called "trench isolation structure" by a selective oxidation method, which forms shallow trenches in the substrate surface and then selectively oxidizes the trench portions to form the thermal oxide film, has been employed in place of the LOCOS structure as the insulation/isolation structure of

semiconductor devices for which high integration density is required, as described in JP-A-63-143835, for example.

In comparison with the LOCOS structure, this trench isolation structure has the advantage that it can form device isolation oxide films having smaller planar dimensions. For this reason, this method is suitable for the fabrication of deep submicron devices for which processing dimensional accuracy of 0.5 um or below is required.

When a silicon thermal oxide film is formed by oxidizing the surface of a silicon substrate as a semiconductor substrate, for example, a large mechanical stress develops near the interface between the thermal oxide film so formed and the silicon substrate. This is because a part of the silicon substrate (Si) is oxidized and undergoes volume expansion of about twice when it changes to the thermal oxide film (SiO_2). When this mechanical stress increases, crystal defects such as dislocation and stacking faults are likely to occur and reliability of the semiconductor devices drops. It has been also clarified that the oxidation reaction itself (diffusion behavior of oxidizing species, reactivity on the oxidation interface, etc) is affected by the stress and the shape of the growing oxide film changes. Since the stress occurs concentratedly near the end points (corner points) of the two-dimensional or three-dimensional shape, careful attention must be paid

particularly to the crystal defects and the shape change in this stress concentration field.

Figs. 1A to 1D are schematic views of a fabrication process of a trench isolation structure in a conventional selective oxidation method. According to the conventional method shown in Fig. 1A, an oxidation prevention film 3 is first deposited to a surface of a silicon substrate 1 through a pad oxide film (silicon thermal oxide film) 2, then the oxidation prevention film 3, the pad oxide film 2 and the silicon substrate 1 of the area, where a device isolation oxide film is desired to be formed, are partially removed to form a trench (Fig. 1B), and the silicon thermal oxide film 5 is formed by oxidizing the trench surface.

Thereafter, a gate oxide film 6, a gate electrode 7, an inter-layer insulating film 8, a buried insulating film 9, a first layer wiring 10 and a second layer inter-layer insulating film 11 are serially formed.

In this trench isolation structure, the end points (corner points) essentially exist near the trench upper end portion or the trench lower end portion of the substrate. Therefore, the stress concentration field is formed near the end point (corner point) due to thermal oxidation. Because such a stress concentration field is formed, the shape of the substrate, particularly near the trench upper end portion, is oxidized in some cases into a pointed shape 4 having an acute angle as shown in

Fig. 1C. After the formation of the device isolation oxide film, an electronic circuit such as transistors, capacitors, etc, is formed in a device formation area covered with the oxide protective film 3 as shown in Fig. 1D. If such an acute angle portion 4 remains on the substrate surface, however, the concentration of electric field occurs at this portion during the circuit operation and deteriorates the breakdown voltage characteristics of the transistors, the capacitances, etc, that constitutes the circuit, as pointed out by A. Bryant et al. in "Technical Digest of IEDM '94", pp. 671-674.

DISCLOSURE OF INVENTION

In semiconductor devices having a trench isolation structure, the present invention is directed to provide a semiconductor device which does not invite deterioration of breakdown voltage characteristics of transistors and capacitances constituting a circuit but has high reliability, and a method of fabricating such a semiconductor device.

The object described above can be accomplished by preventing a substrate shape in the proximity of the upper end portion of a device isolation trench on a surface of a semiconductor substrate from becoming an acute angle.

A method of fabricating a semiconductor device for accomplishing the object described above includes the following steps.

(1) Step to form oxide prevention film on circuit formation surface of semiconductor substrate:

A silicon substrate, etc, may be used as the semiconductor substrate.

The film thickness of the oxidation prevention film must be such that all the oxide prevention films are not oxidized in the oxidation steps of the post-steps (4), (7), etc.

A polycrystalline silicon thin film, a silicon nitride film, etc, may be used as the oxidation prevention film. Since easily oxidizable materials such as the polycrystalline silicon thin film have low restriction force to volume expansion of the new grown silicon oxide film from the silicon substrate with oxidation, the stress concentration at the trench upper end portion can be reduced. Since difficultly oxidizable materials such as the silicon nitride film have a small oxidation quantity in the oxidation process, the film thickness can be reduced.

It is also effective to form a pad oxide film on the silicon substrate before the oxidation prevention film is formed. If the pad oxide film exists, the portions in the proximity of the lower end of the oxidation prevention film and the upper end of the semiconductor substrate that keep contact with the pad

oxide film are sequentially oxidized from the trench end portion, and the so-called "bird's beak" is formed at the contact portion between the pad oxide film and the semiconductor substrate. As a result, the radius of curvature at the corners near the upper end of the semiconductor substrate is promoted.

(2) Step to form trench having predetermined depth at desired positions of circuit formation surface of semiconductor substrate:

This trench can be formed by an ordinary lithography method using a photoresist and etching, for example.

(3) Step to remove corners formed by trench on circuit formation surface of semiconductor substrate:

This step is not always necessary, but if the corners are removed by this step, the oxidation step (7) of the post-step becomes unnecessary in most cases.

(4) Step to oxidize trench portion formed in semiconductor substrate:

The trench portion is oxidized by several to dozens of nm by oxidation. Due to this oxidation, the bird's beak is grown at the trench portion and a radius of curvature is formed at the corners at the trench upper end portion.

(5) Step to bury buried insulating film into oxidized trench:

Preferably, the material used as the buried insulating film is essentially an insulating material

and has a low dielectric constant. For, if a material having a high dielectric constant is used, a coupling capacitance which is formed when a wiring material is deposited on this insulating film at a post-step becomes great. From this aspect, a silicon oxide film, etc, is a preferred burying material, and polycrystalline silicon or the like is not preferred.

(6) Step to remove buried insulating film formed on oxidation prevention film:

The buried insulating film is etched back by chemical-mechanical polishing (CMP) or dry etching. In this case, the oxidation prevention film serves as an etching stopper and has also the function of preventing etching of the semiconductor substrate below the oxidation prevention film.

(7) Step to oxidize semiconductor substrate after removal of buried insulating film formed on oxidation prevention film:

This step grows the radius of curvature of the trench upper end portion of the semiconductor substrate to a sufficient radius of curvature for preventing the increase of the leakage current. This oxidation step provides also the effect that the buried insulating film is made compact.

This step is not necessary if the radius of curvature at the trench upper end portion of the semiconductor substrate has become sufficient to prevent

the increase of the leakage current due to the oxidation step (4).

This step may be executed before the step (6) or the next step (8). When this step is executed after the next step (8), the surface of the semiconductor substrate is simultaneously oxidized, too, but the oxide film formed on the surface of the semiconductor substrate is removed after completion of additional oxidation and in this way, the step of forming the device isolation oxide film is completed.

(8) Step to remove oxidation prevention film formed on circuit formation surface of semiconductor substrate:

The formation step of the device isolation oxide film is completed by this step. Therefore, a semiconductor device is formed by forming a circuit such as transistors on the semiconductor substrate on which the device isolation oxide film is formed.

A semiconductor device according to the present invention for accomplishing the afore-mentioned objects is a semiconductor device having a device isolation oxide film which is formed on a circuit formation surface of a semiconductor substrate and is a trench isolation structure, wherein an angle θ between the circuit formation surface of the semiconductor substrate and the side surface of the semiconductor substrate in a depth-wise direction of the trench constituting the trench isolation structure is within

the range of $90° < \theta < 180°$. Because this structure can prevent field concentration at the trench upper end portion, it can prevent the increase of a leakage current resulting from deterioration of withstand voltage characteristics of the circuit such as transistors and capacitances formed on the semiconductor substrate.

The coupling capacitance of wirings constituted on the semiconductor substrate can be reduced by burying the inside of the trench by an insulating material having a low dielectric constant such as a silicon oxide, and reliability of the semiconductor device can be further improved.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A, 1B, 1C and 1D are schematic views, each showing a fabrication process of a trench isolation structure in a selective oxidation method according to the prior art;

Figs. 2A to 2N are schematic views, each showing a fabrication process of an MOS transistor according to the first embodiment of the present invention;

Fig. 3 is a flowchart showing the fabrication process of the MOS transistor according to the first embodiment of the present invention;

Figs. 4A to 4N are schematic views, each showing a fabrication process of an MOS transistor according to the second embodiment of the present invention;

Fig. 5 is a flowchart showing the fabrication process of the MOS transistor according to the second embodiment of the present invention;

Figs. 6A to 6N are schematic views, each showing a fabrication process of an MOS transistor according to the third embodiment of the present invention;

Fig. 7 is a flowchart of the fabrication process of the MOS transistor according to the third embodiment of the present invention;

Figs. 8A to 8N are schematic views, each showing a fabrication process of an MOS transistor according to the fourth embodiment of the present invention; and

Fig. 9 is a flowchart of the fabrication process of the MOS transistor according to the fourth embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Hereinafter, preferred embodiments of the present invention will be explained with reference to the accompanying drawings.

A fabrication process of an MOS transistor according to the first embodiment of the present invention will be explained with reference to Figs. 2A to 2N and Fig. 3. Figs. 2A to 2N are schematic views of the fabrication process of the MOS transistor according to the first embodiment, and Fig. 3 is a flowchart of the fabrication process of this MOS transistor.

The fabrication process of the MOS transistor of this first embodiment is as follows.

(1) A surface of a silicon substrate 1 is thermally oxidized so as to form a pad oxide film 2 having a thickness of 10 to several tens of nm [Fig. 2B and Fig. 3 (101) to (102)].

(2) A polycrystalline silicon thin film 18 is deposited on the pad oxide film 2 to a thickness of about 10 to 200 nm [Fig. 2B, Fig. (103)]. This polycrystalline silicon thin film 18 is used as an oxidation prevention film when a device isolation thermal oxide film 5 is formed. Incidentally, the polycrystalline silicon film 18 may be directly deposited on the silicon substrate 1 by omitting the formation of the pad oxide film 2.

Incidentally, the following description is based on the assumption that the pad oxide film 2 is formed. Therefore, the process step relating to the pad oxide film 2 is not necessary when the formation of the pad oxide film 2 is omitted.

(3) A photoresist 19 is formed on the polycrystalline silicon film 18 [Fig. 2B, Fig. 3 (104)].

(4) After the photoresist 19 in an area, in which a device isolation film is to be formed, is removed by an ordinary lithography method, a part of each of the polycrystalline silicon thin film 18, the pad oxide film 2 and the silicon substrate 1 is removed by anisotropic etching so as to form a shallow trench whose sidewalls

have a predetermined angle (substantially, about 60 to about 90 degrees) on the surface of the silicon substrate 1 [Figs. 2C to 2D, Fig. 3 (105) to (107)].

(5) After the remaining photoresist 19 is completely removed, thermal oxide is carried out so as to form an oxide film 5 by oxidizing the trench portion formed in the surface of the silicon substrate 1 to several to dozens of nm [Figs. 2E and 2F, Fig. 3 (108) to (109)]. Incidentally, a sufficient film thickness of the polycrystalline silicon thin film 18 deposited as the oxidation prevention film must be secured so that it can function as the oxidation prevention film for preventing the surface side of the polysilicon thin film 18 from being fully oxidized at the time of thermal oxidation and preventing the silicon substrate 1 below this polycrystalline silicon thin film 18 from being oxidized entirely. When this pad oxide film 2 exists, silicon in the proximity of the lower end of the polycrystalline silicon thin film 18 and the upper end of the silicon substrate 1 keeping contact with the pad oxide film 2 is sequentially oxidized from the trench end, and a so-called "bird's beak" is formed between the contact portions. As a result, the radius of curvature in the proximity of the upper end of the silicon substrate 1 is promoted. From this aspect, the pad oxide film 2 is preferably formed.

(6) Because the inside of the trench is not completely buried by this trench oxidation, an

insulating film 9 such as a silicon oxide film is deposited by chemical vapor deposition, sputtering, etc, in order to completely bury the inside of the trench covered by the thermal oxidation film (hereinafter, the insulating film 9 for burying the inside of the trench will be called the "buried insulating film 9") [Fig. 2G, Fig. 3 (110)]. Basically, the material used for this buried insulating film 9 is an insulating material and preferably has a low dielectric constant. For, when a material having a high dielectric constant is used, a coupling capacitance formed when a wiring material is deposited on this film in a post-step becomes greater. From this aspect, it is not preferred to use poly-crystalline silicon as the burying material.

(7) The buried insulating film 9 is then etched back by chemical-mechanical polishing (CMP) or dry etching [Fig. 2G, Fig. 3 (111)]. In this case, the polycrystalline silicon thin film 18 used as the oxidation prevention film functions as an etching stopper and plays the role of preventing the silicon substrate 1 below the polycrystalline silicon thin film 18 from being etched.

(8) When the radius of curvature of the trench upper end portion 12 due to the bird's beak grown between the contact portions by the oxidation of the trench portion of the silicon substrate 1 is sufficient for preventing the increase of the leakage current, the formation step of the device isolation oxide film is

completed by removing the polycrystalline silicon thin film 18 and the pad oxide film 2 [Fig. 2H, Fig. 3 (113)].

When the radius of curvature of the trench upper end portion 12 due to the bird's beak grown by the oxidation of the trench portion of the silicon substrate 1 is not sufficient for preventing the leakage current depending on the product specification for each product, for example, thermal oxidation is again carried out (hereinafter called "additional oxidation") after the buried insulating film 9 is etched back from the next product lot [Fig. 2I, Fig. 3 (112)].

In this case, since the buried insulating film 9 has already been formed inside the trench of the silicon substrate 1, oxidation proceeds from near the trench upper end portion 12 and the inside of the trench is hardly oxidized for the following reason. In other words, though the inside of the trench is to be thermally oxidized through the buried insulating film 9, a longer time is necessary for the oxidation seeds to diffuse inside the buried insulating film 9 before reaching the silicon substrate 1 than when the silicon substrate is directly oxidized. Therefore, oxidation hardly proceeds substantially within a short period of several minutes near the bottom of the trench. On the other hand, a weak boundary layer of the coupling portion deposited by chemical vapor deposition or sputtering to the trench sidewalls and the upper surface

of the trench exists at the trench upper end portion 12, and the oxidation seeds can diffuse at a relatively high rate along this weak boundary layer. As a result, the oxidation seeds are supplied to the trench upper end portion 12 within a short time (10 or more minutes at the oxidation temperature of 850°C), so that only the portions in the proximity of the trench upper end portion 12 are oxidized preferentially and the formation of the radius of curvature of the trench upper end portion 12 is promoted.

Furthermore, this additional oxidation provides the effect of rendering the buried insulating film 9 compact. After this additional oxidation is completed, the formation step of the device isolation oxide film is completed by removing the polycrystalline silicon thin film 18 and the pad oxide film 2 [Fig. 2M, Fig. 3 (113)].

This additional oxidation may be carried out after the polycrystalline silicon thin film 18 is removed. In this case, the surface of the silicon substrate 1 is simultaneously oxidized, too, but the formation step of the device isolation oxide film is completed by removing this oxide film formed on the surface of the silicon substrate 1 after the additional oxidation is completed.

(9) Transistor structures, etc, are formed on the silicon substrate 1 [Figs. 2J, K, L, N(h), Fig. 3 (114) to (122)].

Conventional fabrication technologies of the transistor structure, etc, can be employed without particular limitation, and a typical fabrication proces of the MOS transistor structure will be explained next by way of example.

(a) Any of a silicon oxide film, a silicon nitride film, an acid nitride film and a high dielectric thin film (insulating films of a higher dielectric constant than SiO_2 such Ta_2O_5, PZT, and BsT), or their laminate body, is formed as the gate oxide film 6 on the silicon substrate 1.

These thin films can be formed by CVD, or the like, for example. The silicon oxide film may be formed by thermal oxidation of the silicon substrate 1.

(b) Any of a polycrystalline silicon thin film, a metal thin film such as a tungsten film and a silicide thin film, or their laminate body, is formed, and then unnecessary portions are removed by etching, etc, to form a gate electrode 7.

(c) An impurity is implanted and a first layer wiring 10, an inter-layer insulating film 11, etc, are formed.

Further, an inter-layer insulating film 14, a wiring 15 and an insulting film 16 are formed, whenever necessary.

The MOS transistor described above can be used for memory circuits such as a DRAM (Dynamic Random

Access Memory) or arithmetic operation circuits such as logic devices.

The first embodiment described above can prevent the acute angle portions from remaining near the trench upper end portions of the silicon substrate when the trench isolation structure is formed as the device isolation oxide film structure, can prevent the increase of the leakage current or the drop of withstand voltage characteristics of the MOS transistor resulting from the field concentration in the proximity of the gate electrode film, by forming the radius portions or the obtuse angle portions near the trench upper end portion of the silicon substrate, and can improve electrical reliability of the transistor.

Incidentally, since the trench upper end portion of the silicon substrate before thermal oxidation is substantially orthogonal in the first embodiment, there is the case where the radius of curvature near the trench upper end portion of the silicon substrate is not sufficient. However, because polycrystalline silicon as the oxidation prevention film is easily oxidized, the restriction force to the volume expansion of the newly grown silicon oxide from the silicon substrate is lower in comparison with those materials which are difficultly oxidized, and there is sometimes the case where additional oxidation is not necessary. Furthermore, processing of the trench is

easy and this embodiment is excellent in the aspect of productivity, too.

Next, the fabrication process of an MOS transistor according to the second embodiment of the present invention will be explained with reference to Figs. 4A to 4N and Fig. 5. Figs. 4A to 4N are schematic views showing the fabrication process of the MOS transistor according to the second embodiment, and Fig. 5 is a flowchart of the fabrication process of the MOS transistor of this embodiment.

The fabrication process of the MOS transistor of the second embodiment modifies the fabrication step (4) of the first embodiment in the following way. Since the fabrication steps other than the step (4) are the same as those of the first embodiment, the detailed explanation will be omitted.

(4) After the photoresist 19 of the area in which the device isolation film is to be formed is removed by an ordinary exposure method, a part of each of the polycrystalline silicon thin film 18, the pad oxide film 2 and the silicon substrate 1 is removed by etching, and a shallow trench is formed in the surface of the silicon substrate 1. When forming the trench in the surface of the silicon substrate, isotropic etching is applied near the trench upper end portion so as to form the radius of curvature near the trench upper end portion, and then anisotropic etching is applied so as to define the trench shape having the slope portion like the isotropic

etching portion 13. Incidentally, the angle of the trench sidewalls near the trench lower end portion need not always be 90 degrees and a predetermined inclination (substantially within the range of 60 to 90 degrees) [Figs. 4C, D, E, Fig. 5 (205) to (207)] may be formed.

In comparison with the second embodiment, the etching step, that is, isotropic etching and anisotropic etching, at the time of formation of the shallow trench becomes more complicated. However, because the isotropic etching portion 13 is disposed at the trench upper end portion of the silicon substrate at the time of formation of the shallow trench as described above, oxidation of the trench upper end portion of the silicon substrate 1 by first thermal oxidation (formation of the radius of curvature) is promoted, and the necessity for additional oxidation becomes lower.

Next, the fabrication process of an MOS transistor according to the third embodiment of the present invention will be explained with reference to Figs. 6A to 6N and Fig. 7. Figs. 6A to 6N are schematic views of the fabrication process of the MOS transistor according to the third embodiment and Fig. 7 is a flowchart of the fabrication process of the MOS transistor of this embodiment.

The fabrication process of the MOS transistor according to the third embodiment is as follows.

(1) The surface of the silicon substrate 1 is thermally oxidized and the pad oxide film 2 having a

thickness of 10 to dozens of nm is formed [Figs. 6B, Fig. 7 (301) to (302)].

(2) A silicon nitride film 17 having high oxidation resistance is deposited to a thickness of 10 to 200 nm on the pad oxide film 2 [Fig. 6B, Fig. 7 (303)]. This silicon nitride film 17 is used as an oxidation prevention film when the device isolation oxide film 5 is formed. Incidentally, the silicon nitride film 17 having high oxidation resistance may be directly formed on the silicon substrate 1 by omitting the formation of the pad oxide film 2. Alternatively, the silicon nitride film 17 is deposited through the pad oxide film 2 and te polycrystalline silicon thin film, or through only the polycrystalline silicon thin film. In either case, the silicon nitride film 17 exists on the outermost surface of the structure.

Incidentally, the following description is based on the assumption that the polycrystalline silicon thin film and the pad oxide film 2 are formed. Therefore, when the formation of the polycrystalline silicon thin film and the pad oxide film 2 is omitted, the process steps relating to the polycrystalline silicon thin film and the pad oxide film 2 are not necessary.

(3) The photoresist 19 is formed on the silicon nitride film 17 [Fig. 6B, Fig. 7 (304)].

(4) After the photoresist 19 of the area in which the device isolation film is to be formed is removed by

an ordinary lithography method, the silicon nitride film 17, the pad oxide film 2 and the polycrystlaline silicon film are removed by etching. Next, the photoresist is removed, and the shallow trench is formed in the surface of the silicon substrate 1 by dry etching. When this trench is formed in the surface of the silicon substrate, isotropic etching is applied to the portions near the trench end portion so as to form the radius of curvature in the proximity of the trench upper end and then anisotropic etching is applied to form the trench shape having the slope portion like the isotropic etching portion 13. Incidentally, the angle of the trench sidewalls near the trench lower end portion need not always be 90 degrees, and a predetermined inclination (substantially within the range of 60 to 90 degrees) may be formed, as well [Figs. 6C, D, E, Fig. 7 (305) to (308)].

(5) After the photoresist 9 is removed, thermal oxidation is carried out to oxidize the trench portion formed in the surface of the silicon substrate 1 to a thickness of several to dozens of nm [Figs. 6E, D, F, Fig. 7 (309)]. Incidentally, the film thickness of the silicon nitride film 17 as the oxidation prevention film must be a film thickness sufficient to function as the oxidation prevention film to prevent the silicon nitride film 17 from being completely oxidized at the time of thermal oxidation and to prevent the silicon substrate 1 below the silicon nitride film 17 from being completely

oxidized. Since this silicon nitride film 17 has high oxidation resistance, the film thickness can be made thinner than the polycrystalline silicon thin film 18 used in the first and second embodiments. When the pad oxide film 2 exists, silicon in the proximity of the upper end portion of the silicon substrate 1 keeping contact with the pad oxide film 2 and the lower end of the polycrystalline thin film are serially oxidized from the trench end, and the so-called "bird's beak" is formed, so that the radius of curvature near the upper end of the silicon substrate 1 is promoted. From this aspect, the pad oxide film 1 is preferably formed.

(6) Since the inside of the trench is not fully buried by this trench oxidation, the insulating film 9 such as a silicon oxide film is deposited to bury the inside of the trench by chemical vapor deposition, sputtering, etc, in order to fully bury the inside of the trench covered by the thermal oxidation film (hereinafter, the insulating film 9 for burying the inside of the trench will be called the "buried insulating film 9") [Fig. 6G, Fig. 7 (310)].

Fundamentally, the material used for the burying insulating film 9 is preferably a material having an insulating property and a low dielectric constant. For, when a material having a high dielectric constant is used, a coupling capacitance formed when a wiring material is deposited on the film material in the post-process becomes great. From this aspect, the use

of polycrystalline silicon as the burying material is not preferred.

(7) When the radius of curvature at the trench upper end portion due to the bird's beak grown by the oxidation of the trench portion of the silicon substrate 1 is sufficient to prevent the increase of the leakage current, the formation process of the device isolation oxide film is completed by etching back the buried insulating film 9 and then removing the remaining silicon nitride film 17, polycrystalline silicon and pad oxide film 2 [Figs. 6H, I, Fig. 7 (313)].

When the radius of curvature of the trench upper end portion due to the bird's beak grown by the oxidation of the trench portion of the silicon substrate 1 is not sufficient for preventing the increase of the leakage current, thermal oxidation is again carried out (hereinafter called "additional oxidation") before the buried insulating film 9 is etched back [Fig. 6L, Fig. 7 (312)].

In this case, since the buried insulating film 9 has already been formed inside the trench of the silicon substrate 1, oxidation proceeds from portions near the trench upper end portion 12 and the inside of the trench is hardly oxidized for the following reason.

In other words, thermal oxidation inside the trench is carried out through the buried insulating film 9 but in this case, a longer time is necessary for the oxidation seeds to diffuse inside the buried insulating

film 9 before reaching the silicon substrate 1 than when the silicon substrate is directly oxidized. Therefore, oxidation does not substantially proceed within a short time of several minutes near the bottom of the trench. On the other hand, a weak boundary layer of the coupling portion of the buried insulating film 9 deposited to the trench sidewalls and the trench upper surface by chemical vapor deposition or sputtering exists at the trench upper end portion 12. Accordingly, the oxidation seeds can diffuse at a relatively high rate along this weak boundary layer, so that the oxidation seeds are supplied to the trench upper end portion 12 within a short time (10 minutes or more at an oxidation temperature of 850°C), the portions near the trench upper end portion 12 are oxidized preferentially and the formation of the radius of curvature of the trench upper end portion 12 is promoted.

When the radius of curvature of the trench upper end portion 12 due to the bird's beak grown by this additional oxidation is sufficient to prevent the increase of the leakage current, the formation process of the device isolation oxide film is completed by etching back the buried insulating film 9 and then removing the remaining silicon nitride film 17, polycrystalline silicon and pad oxide film 2 [Fig. 6M, Fig. 7 (313)].

Incidentally, this additional oxidation need not always be carried out before etch-back of the buried

insulating film 9, and may be carried out after etch-back of the buried insulating film 9 in accordance with the product specification required for products in the same way as in the first embodiment.

(8) A transistor structure, etc, is formed on the silicon substrate 1 [Figs. 6J to 6N, Fig. 7 (314) to (322)].

Conventional fabrication technologies of the transistors can be employed without particular limitation, and the explanation will be given on a typical fabrication process of the MOS transistor structure by way of example.

(a) Any one of a silicon oxide film, a silicon nitride film, an acid nitride film and a high dielectric thin film, or their laminate body, is formed as the gate oxide film 6 on the silicon substrate 1.

These thin films can be formed by CVD, for example. The silicon oxide film may be formed by the thermal oxidation of the silicon substrate 1.

(b) After any of a polycrystalline silicon thin film, a metal film such as a tungsten film and a silicide thin film, or their laminate body, is formed, unnecessary portions are removed by etching, etc, to form the gate electrode 7.

(c) An impurity is implanted and a first layer wiring 10, an inter-layer insulating film 11, etc, are formed. Wirings of the second layer et seq, and an insulating film are formed further, whenever necessary.

The MOS transistor described above can be used for memory circuits such as a DRAM (Dynamic Random Access Memory), an SRAM or arithmetic operation circuits such as logic devices (Static Random Access Memory), etc.

In the fabrication process of the MOS transistor, the third embodiment prevents the acute angle portions from remaining in the proximity of the trench upper end portion of the silicon substrate when forming the trench isolation structure as the device isolation oxide film structure but forms the radius of curvature portion or the obtuse angle portion near the trench upper end portion of the silicon substrate. Therefore, this embodiment can prevent the increase of the leakage current of the MOS transistor or the drop of the breakdown voltage characteristics resulting from the field concentration near the end portion of the gate electrode, and can improve electrical reliability of the transistor.

Incidentally, since the third embodiment uses the silicon nitride film 17 having high oxidation resistance as the oxidation prevention film, the film thickness of the oxidation prevention film can be reduced, and removal of this oxidation prevention film in the final process step becomes easier.

The etching process at the time of the formation of the shallow trench gets complicated in this third embodiment in the same way as in the second

embodiment, but because the isotropic etching portion 13 is disposed at the trench upper end portion of the silicon substrate 1 when the shallow trench is formed as described above, oxidation of the trench upper end portion of the silicon substrate 1 is promoted in the initial thermal oxidation process and the necessity for additional oxidation becomes lower.

Next, the fabrication process of an MOS transistor according to the fourth embodiment of the present invention will be explained with reference to Figs. 8A to 8N and Fig. 9. Figs. 8A to 8N are schematic views of the fabrication process of the MOS transistor of the fourth embodiment and Fig. 9 is a flowchart of the fabrication process of the MOS transistor in this embodiment.

The fabrication process of the MOS transistor of the fourth embodiment modifies the fabrication step (4) of the first embodiment in the following way. Since the fabrication steps other than the step (4) are the same as those of the first embodiment, the detailed explanation will be omitted.

(4) After the photoresist in the area in which the device isolation film is to be formed is removed by an ordinary lighography method, the silicon nitride film 17, the pad oxide film 2 and the polycrystalline silicon thin film are removed by etching. Next, the photoresist is removed and the shallow trench is formed in the surface of the silicon substrate 1 by dry etching. The

angle of the trench sidewalls near the trench lower end portion need not always be 90 degrees and a predetermined inclination (substantially within the range of 760 to 90 degrees) may be formed [Figs. 8C, D, E, Fig. 9 (405) to (408)].

Since the fourth embodiment uses the silicon nitride film 17 having high oxidation resistance as the oxidation prevention film in the same way as in the third embodiment, the film thickness of the oxidation prevention film can be reduced, and removal of the oxidation prevention film in the final process step becomes easier.

The fourth embodiment can easily form the trench by anisotropic etching alone, and has high productivity.

INDUSTRIAL APPLICABILITY

In the semiconductor devices having the trench isolation structure, the embodiments of the present invention can provide a semiconductor device which does not invite deterioration of the transistors constituting the circuit and the breakdown voltage characteristics of the capacitance, and a method of fabricating the semiconductor device.

CLAIMS

1. A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of said semiconductor substrate;

(c) oxidizing said trench portion formed in said semiconductor substrate;

(d) burying a buried insulating film into said trench so oxidized;

(e) removing said buried insulating film formed on said oxidation prevention film; and

(f) removing said oxidation prevention film formed on the circuit formation surface of said circuit substrate.

2. A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming shallow trenches having a radius of curvature at corners in a desired position of the circuit formation surface of said semiconductor substrate;

(c) forming a trench having a predetermined depth to said shallow trenches having a radius of curvature so formed;

(d) oxidizing said trench portions formed in said semiconductor substrate;

(e) burying a buried insulating film into said trenches so oxidized;

(f) removing said buried insulating film formed on said oxidation prevention film; and

(g) removing said oxidation prevention film formed on the circuit formation surface of said semiconductor substrate.

3. A method of fabricating a semiconductor device according to claim 2, wherein said step for forming shallow trenches is carried out by isotropic etching and said step for forming a trenches having a predetermined depth is carried out by anisotropic etching.

4. A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming trenches having a predetermined depth at desired positions of the circuit formation surface of said semiconductor substrate;

(c) oxidizing said trench portions formed in said semiconductor substrate;

(d) burying a buried insulating film into said trenches so oxidized;

(e) removing said buried insulating film formed on said oxidation prevention film;

(f) oxidizing said semiconductor substrate

after said buried insulating film formed on said oxidation prevention film is removed; and

(g) removing said oxidation prevention film formed on the circuit formation surface of said semiconductor substrate.

5. A method of fabricating a semiconductor substrate comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor;

(b) forming shallow trenches having a radius of curvature at corners in desired positions of the circuit formation surface of said semiconductor substrate;

(c) forming trenches having a predetermined depth in said shallow trenches having a radius of curvature;

(d) oxidizing said trench portions formed in said semiconductor substrate;

(e) burying a buried insulation film into said trenches so oxidized;

(f) removing said buried insulating film formed on said oxidation prevention film;

(g) oxidizing said semiconductor substrate after said buried insulating film formed on said oxidation prevention film is removed; and

(h) removing said oxidation prevention film formed on the circuit formation surface of said semiconductor substrate.

6. A method of fabricating a semiconductor device according to claim 5, wherein said step for forming shallow trenches is carried out by isotropic etching and said step for forming a trenches having a predetermined depth is carried out by anisotropic etching.

7. A semiconductor device of the type wherein a device isolation oxide film structure formed on a circuit formation surface of a semiconductor substrate is a trench isolation structure, characterized in that an an angle θ of a trench, which constitutes said trench isolation structure with the circuit formation surface of said semiconductor substrate, in a depth-wise direction with respect to the side surface of said semiconductor substrate is within the range of $90° < \theta < 180°$.

8. A semiconductor device of the type wherein a device isolation oxide film structure formed on a circuit formation surface of a semiconductor substrate is a trench isolation structure, characterized in that an angle θ of a trench, which constitutes said trench isolation structure with the circuit formation surface of said semiconductor substrate, in a depth-wise direction with respect to the side surface of said semiconductor substrate is within the range of $90° < \theta < 180°$, and a silicon oxide exists inside said trench.

FIG. 1A
PRIOR ART

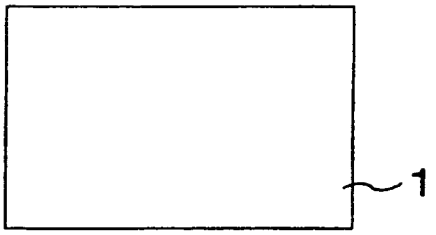


FIG. 1B
PRIOR ART

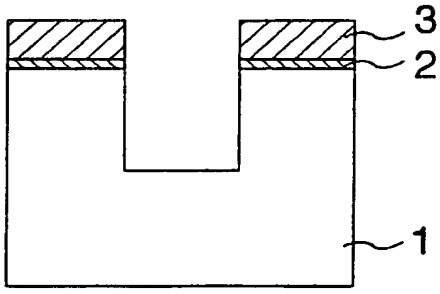


FIG. 1C
PRIOR ART

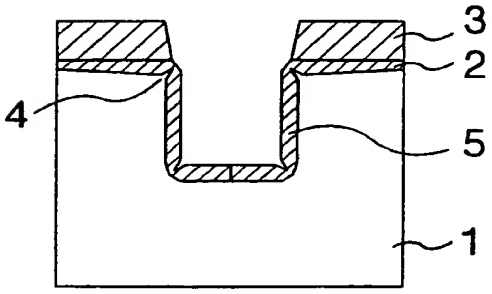


FIG. 1D
PRIOR ART

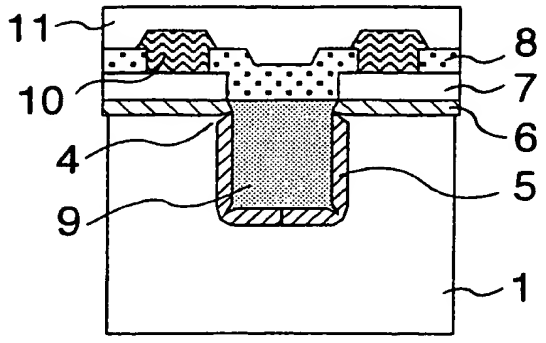


FIG. 2A

FIG. 2B

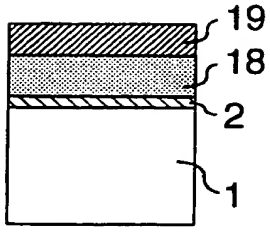


FIG. 2C

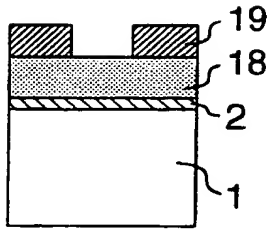


FIG. 2D

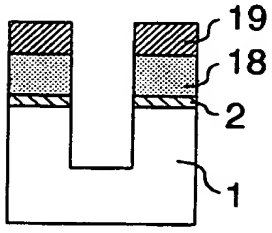


FIG. 2E

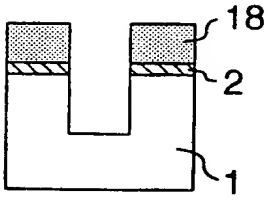


FIG. 2F

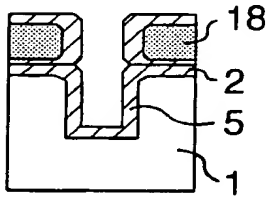


FIG. 2G

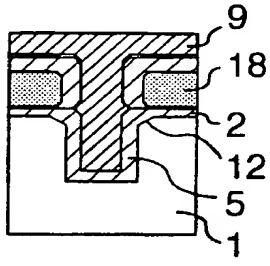


FIG. 2H

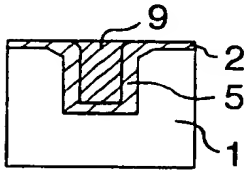


FIG. 2I

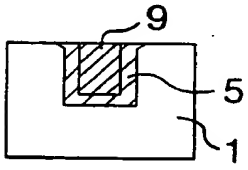


FIG. 2J

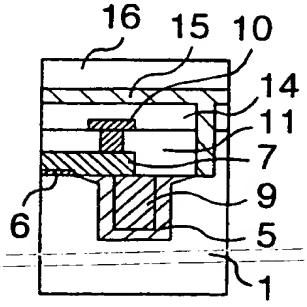


FIG. 2K

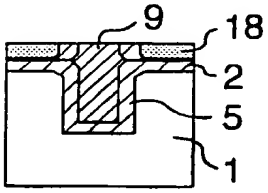


FIG. 2L

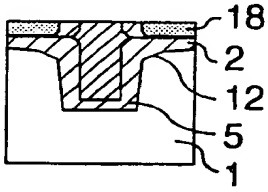


FIG. 2M

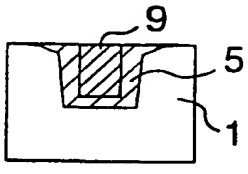


FIG. 2N

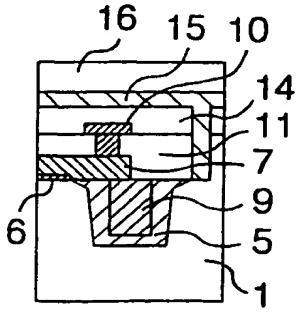
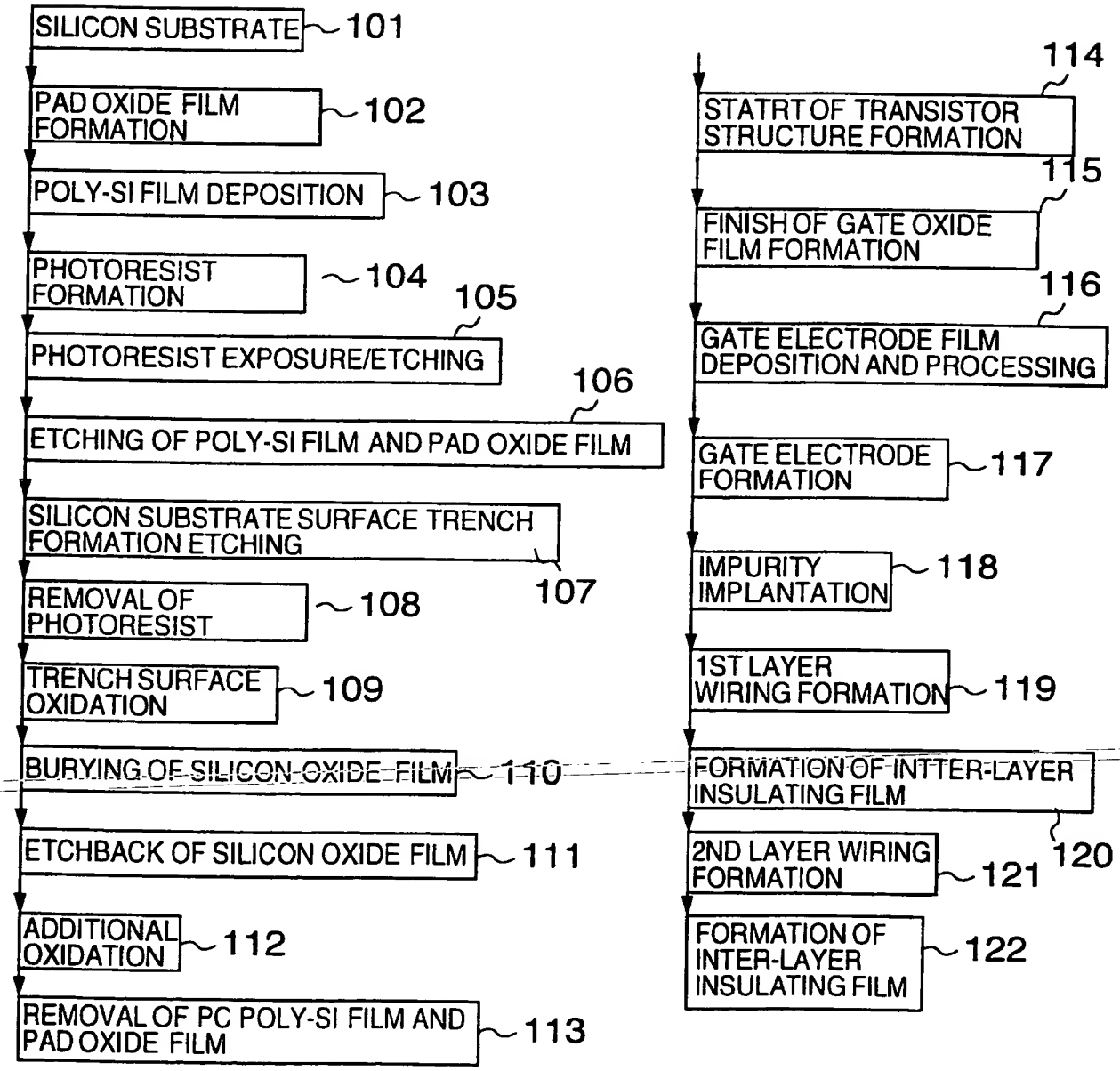


FIG. 3


SILICON SUBSTRATE
101
PAD OXIDE FILM FORMATION
102
POLY-SI FILM DEPOSITION
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PHOTORESIST FORMATION
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PHOTORESIST EXPOSURE/ETCHING
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ETCHING OF POLY-SI FILM AND PAD OXIDE FILM
SILICON SUBSTRATE SURFACE TRENCH FORMATION ETCHING
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FORMATION OF INTTER-LAYER INSULATING FILM
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2ND LAYER WIRING FORMATION
121
FORMATION OF INTER-LAYER INSULATING FILM
122

FIG. 4A

FIG. 4B

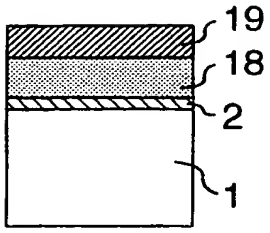


FIG. 4C

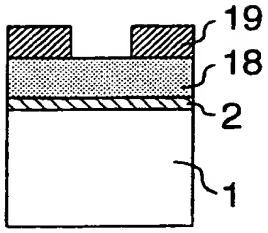


FIG. 4D

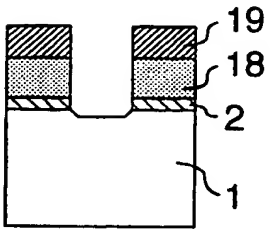


FIG. 4E

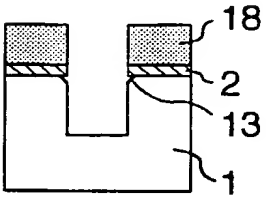


FIG. 4F

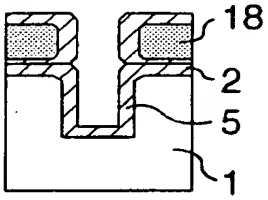


FIG. 4G

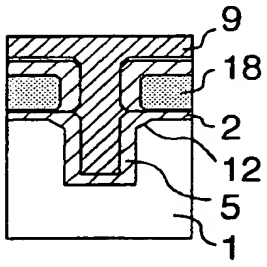


FIG. 4H

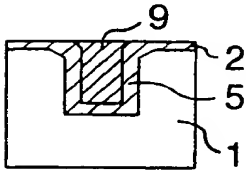


FIG. 4I

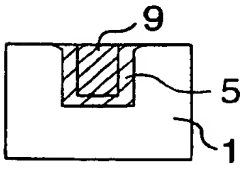


FIG. 4J

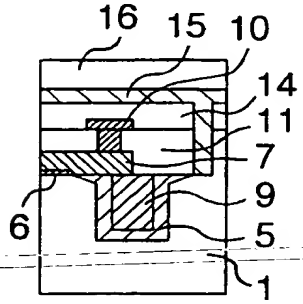


FIG. 4K

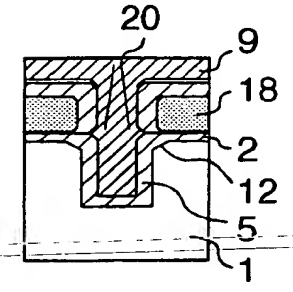


FIG. 4L

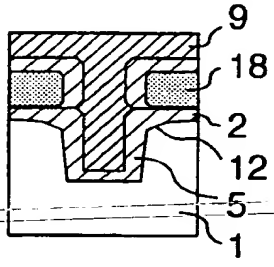


FIG. 4M

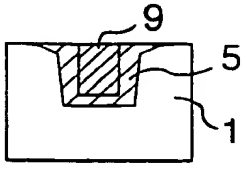


FIG. 4N

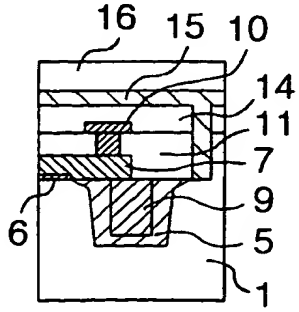
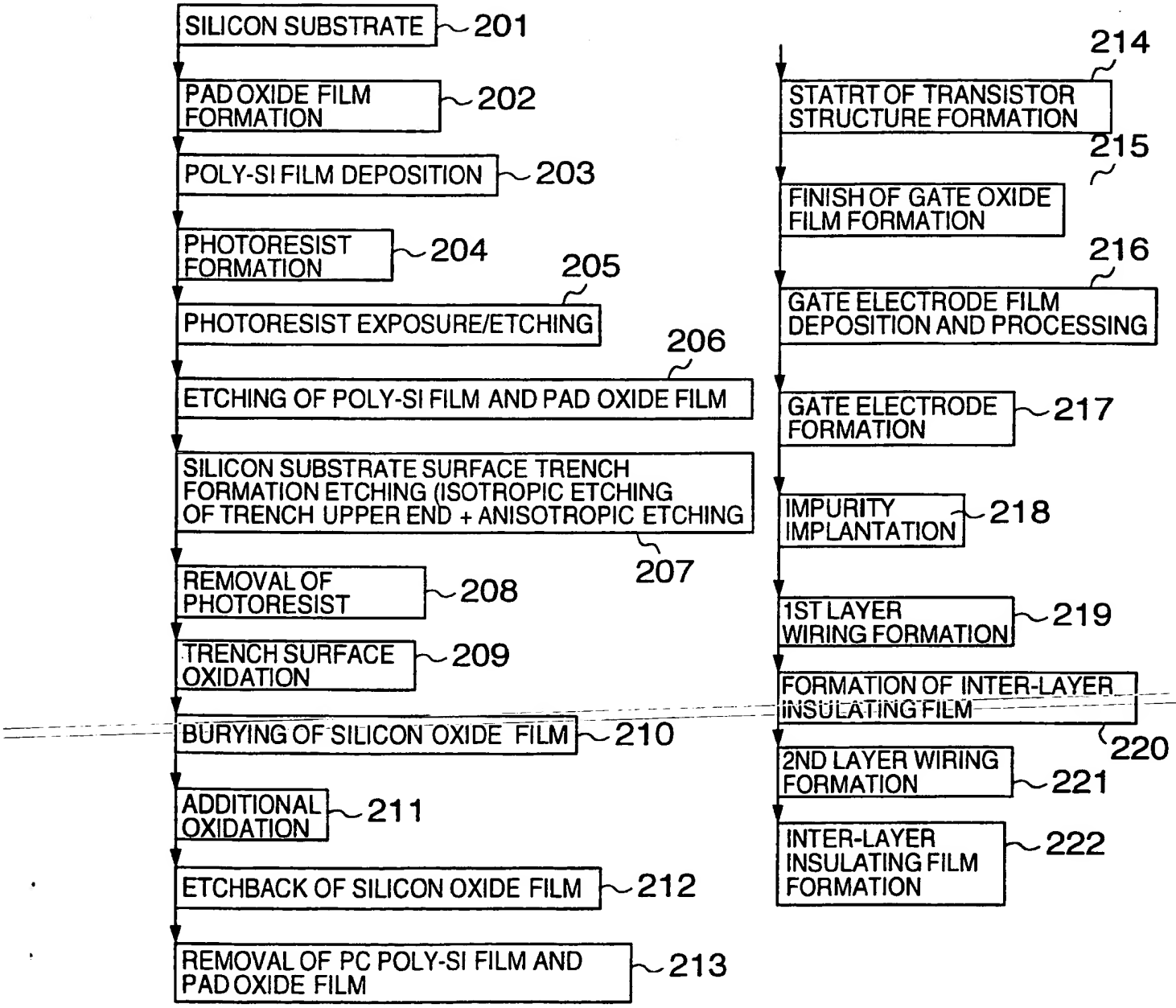


FIG. 5


SILICON SUBSTRATE
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PAD OXIDE FILM FORMATION
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POLY-SI FILM DEPOSITION
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PHOTORESIST EXPOSURE/ETCHING
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ETCHING OF POLY-SI FILM AND PAD OXIDE FILM
SILICON SUBSTRATE SURFACE TRENCH FORMATION ETCHING (ISOTROPIC ETCHING OF TRENCH UPPER END + ANISOTROPIC ETCHING
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REMOVAL OF PC POLY-SI FILM AND PAD OXIDE FILM
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FORMATION OF INTER-LAYER INSULATING FILM
220
2ND LAYER WIRING FORMATION
221
INTER-LAYER INSULATING FILM FORMATION
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FIG. 6A

FIG. 6B

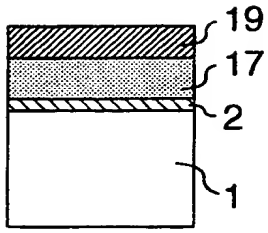


FIG. 6C

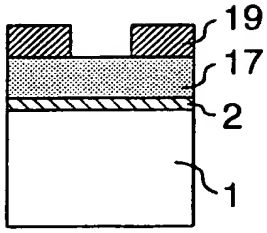


FIG. 6D

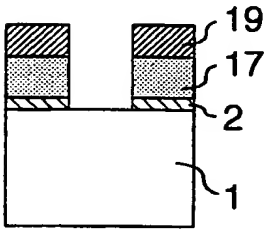


FIG. 6E

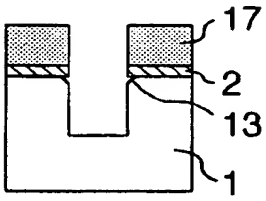


FIG. 6F

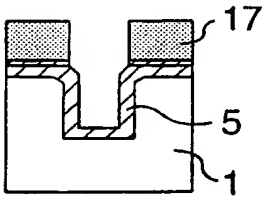


FIG. 6G

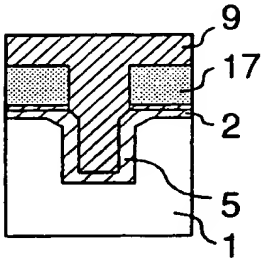


FIG. 6H

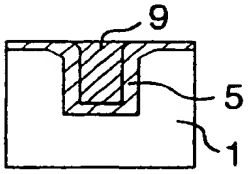


FIG. 6I

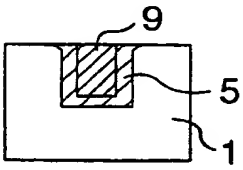


FIG. 6J

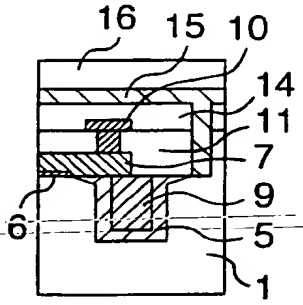


FIG. 6K

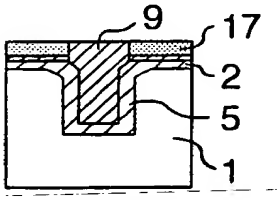


FIG. 6L

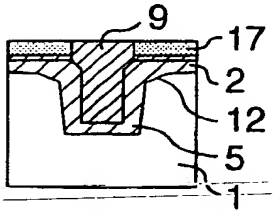


FIG. 6M

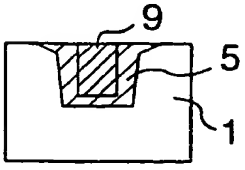


FIG. 6N

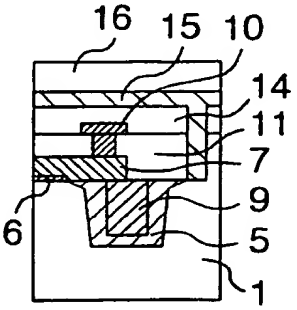
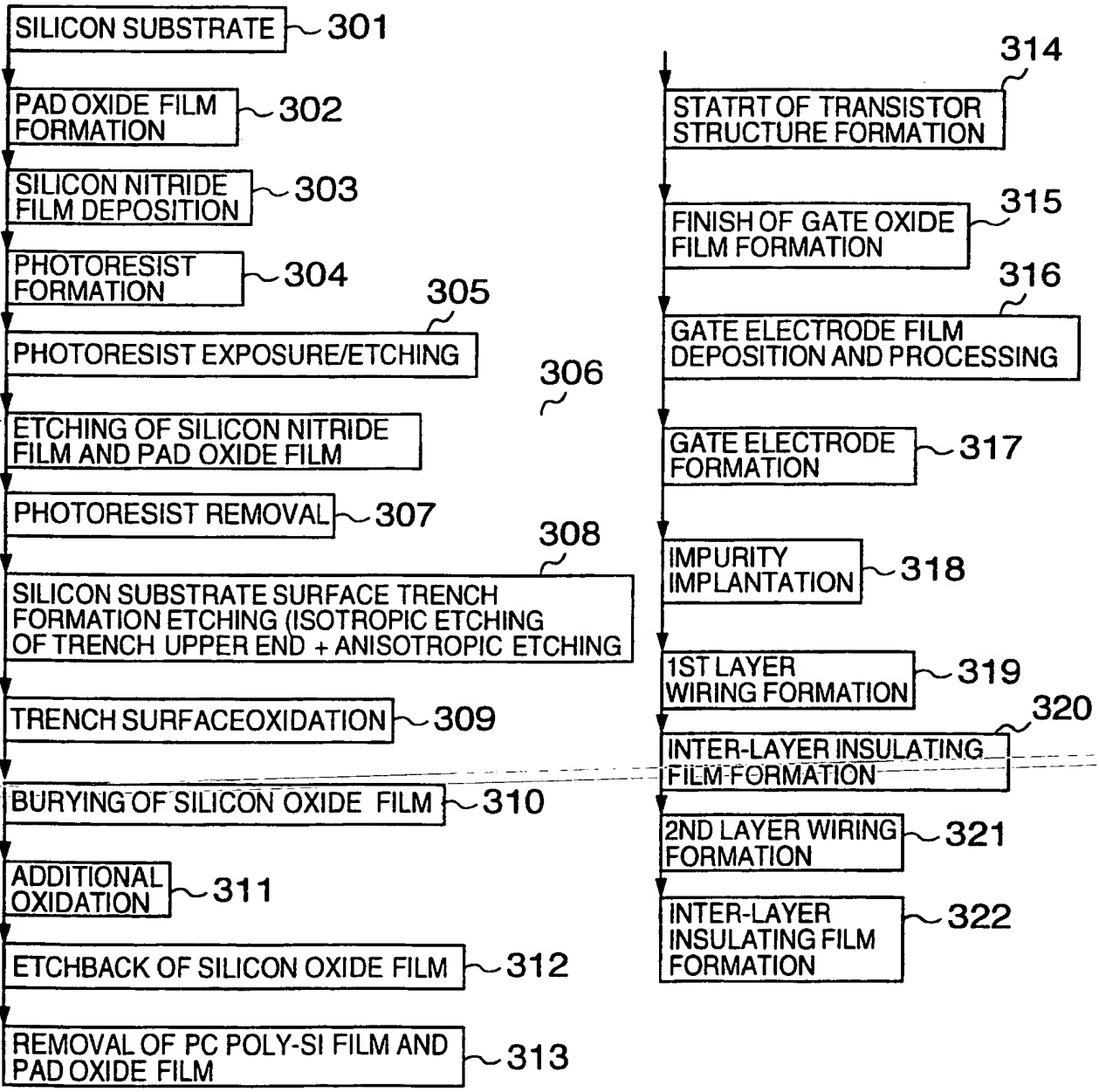


FIG. 7


SILICON SUBSTRATE
301
PAD OXIDE FILM FORMATION
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2ND LAYER WIRING FORMATION
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INTER-LAYER INSULATING FILM FORMATION
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FIG. 8A

FIG. 8B

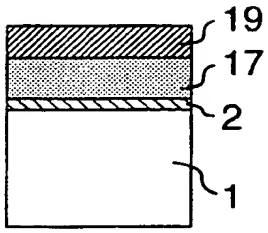


FIG. 8C

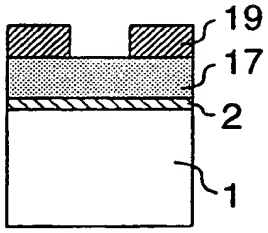


FIG. 8D

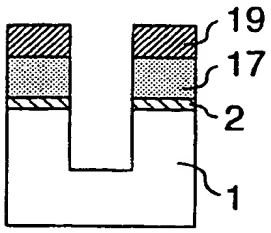


FIG. 8E

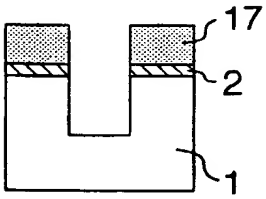


FIG. 8F

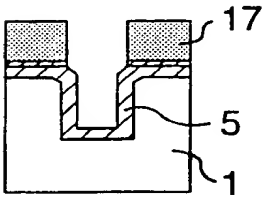


FIG. 8G

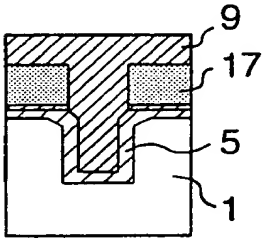


FIG. 8H

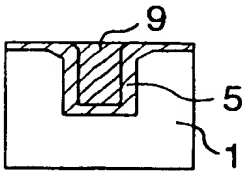


FIG. 8I

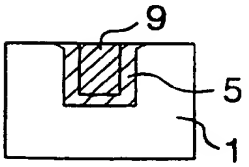


FIG. 8J

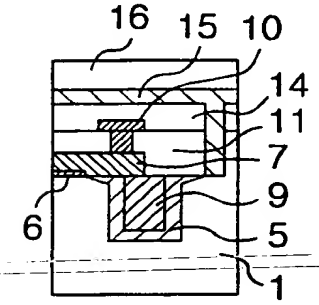


FIG. 8K

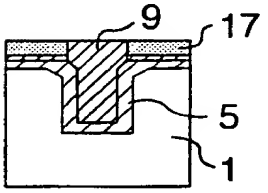


FIG. 8L

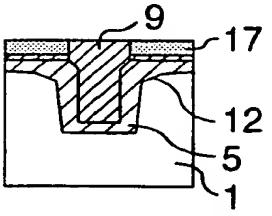


FIG. 8M

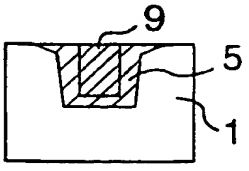


FIG. 8N

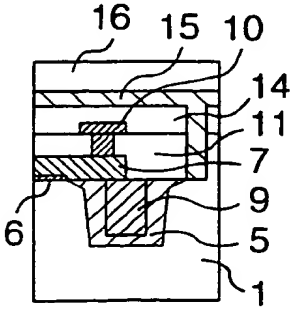
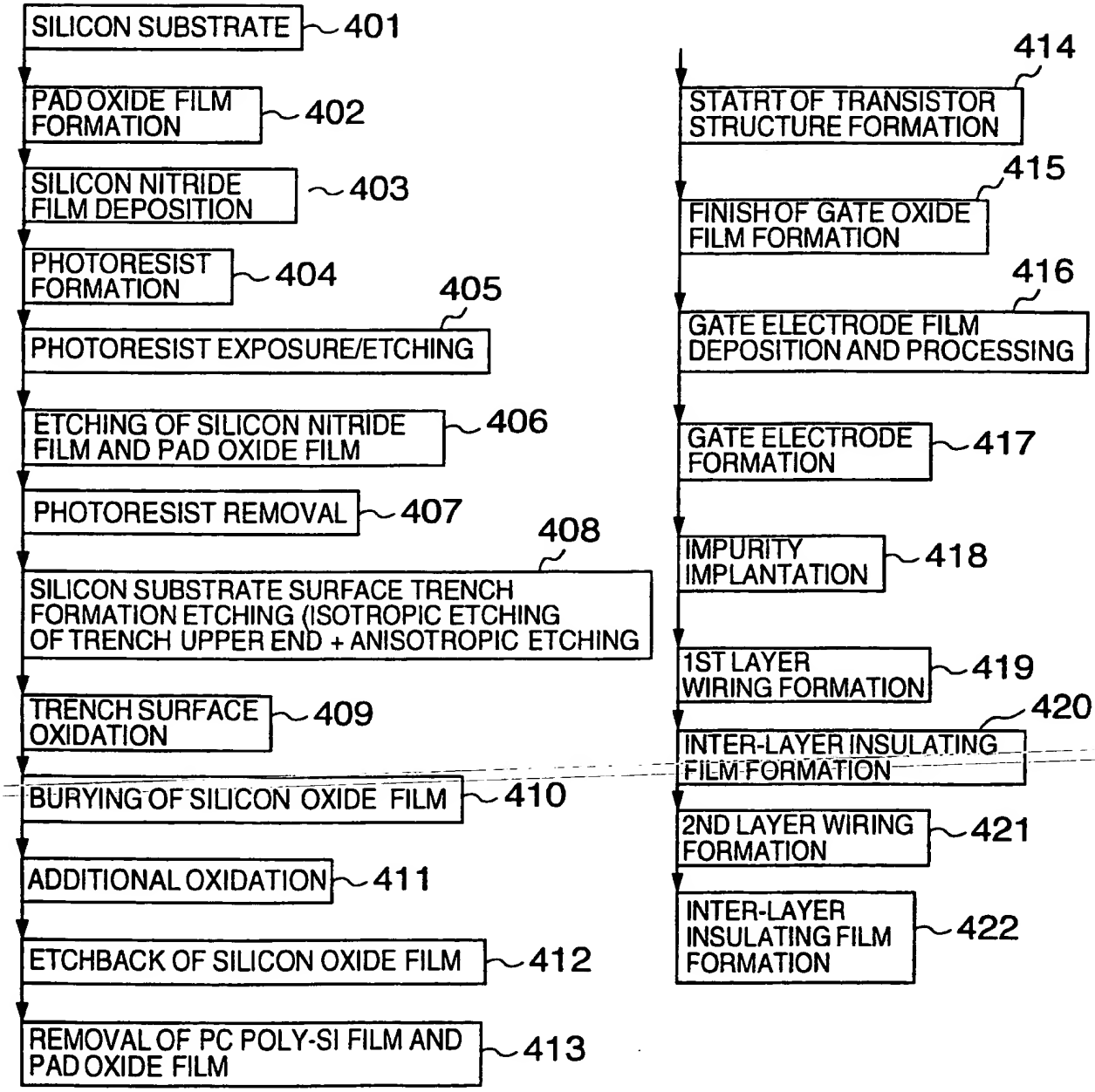


FIG. 9


SILICON SUBSTRATE
401
PAD OXIDE FILM FORMATION
402
SILICON NITRIDE FILM DEPOSITION
403
PHOTORESIST FORMATION
404
405
PHOTORESIST EXPOSURE/ETCHING
ETCHING OF SILICON NITRIDE FILM AND PAD OXIDE FILM
406
PHOTORESIST REMOVAL
407
408
SILICON SUBSTRATE SURFACE TRENCH FORMATION ETCHING (ISOTROPIC ETCHING OF TRENCH UPPER END + ANISOTROPIC ETCHING
TRENCH SURFACE OXIDATION
409
BURYING OF SILICON OXIDE FILM
410
ADDITIONAL OXIDATION
411
ETCHBACK OF SILICON OXIDE FILM
412
REMOVAL OF PC POLY-SI FILM AND PAD OXIDE FILM
413
414
STATRT OF TRANSISTOR STRUCTURE FORMATION
415
FINISH OF GATE OXIDE FILM FORMATION
416
GATE ELECTRODE FILM DEPOSITION AND PROCESSING
GATE ELECTRODE FORMATION
417
IMPURITY IMPLANTATION
418
1ST LAYER WIRING FORMATION
419
420
INTER-LAYER INSULATING FILM FORMATION
2ND LAYER WIRING FORMATION
421
INTER-LAYER INSULATING FILM FORMATION
422

INTERNATIONAL SEARCH REPORT

Inter[redacted] Application No
PCT/JP 97/03267

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/762

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 536 675 A (BOHR MARK T) 16 July 1996 see column 5, line 11 - column 8, line 6; figures 1,3A-3E	1,2
Y	see column 5, line 26 - line 31	3,6
Y	---	4,5
Y	US 5 236 861 A (OTSU TAKAJI) 17 August 1993 see column 3, line 43 - column 4, line 58; figures 3A-3F	4,5

Y	EP 0 459 397 A (TOKYO SHIBAURA ELECTRIC CO) 4 December 1991 see column 2, line 39 - column 3, line 16; figures 2A-2H	3,6

	-/--	

[X] Further documents are listed in the continuation of box C. [X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
8 December 1997	19/12/1997

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Vancraeynest, F

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INTERNATIONAL SEARCH REPORT

Interr[redacted]Application No
PCT/JP 97/03267

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 839 306 A (WAKAMATSU HIDETOSHI) 13 June 1989 see column 1, line 57 - column 3, line 11; example 1E	7,8
A	US 5 316 965 A (PHILIPOSSIAN ARA ET AL) 31 May 1994 see column 3, line 27 - column 4, line 64; figures 5-7	1,4
A	EP 0 660 391 A (TOKYO SHIBAURA ELECTRIC CO) 28 June 1995 see figures 6A-7	1,2

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter[redacted] Application No
PCT/JP 97/03267

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